PATENT

AMENDMENTS TO THE SPECIFICATION

Please replace the first paragraph on page 8 with the paragraph shown below:

-- In the next steps, referring to Fig. 3b, a second insulation layer 51 is grown or deposited over the structure of Fig. 3a in order to insulate the floating gates from a second layer of poly-silicon 52 deposited over the entire area. Next, referring to Fig. 3c, the second poly-silicon layer 52 is patterned and etched to define the two control gates, 54 and 56, and the erase gate 58. In the next step, referring to Fig. 3d, the respective drain regions ~~58~~59 and 60, are formed. The processing steps described above show the fabrication of the transistor pair illustrated in Fig. 2.--

F1

AMENDMENTS TO THE DRAWINGS:

A marked up sheet for sheet #2, which includes the proposed changes to Fig. 3d, is submitted as part of this amendment for the Examiner's review.